

2/12

FIG.1E

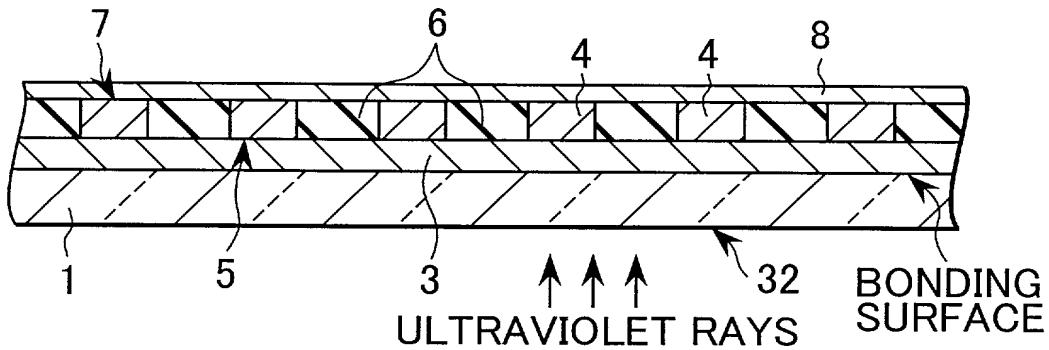


FIG.1F

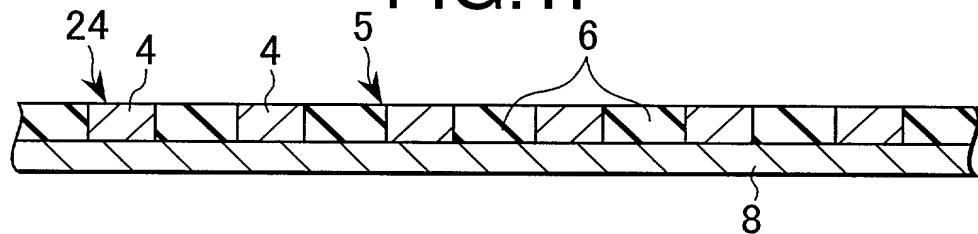


FIG.1G

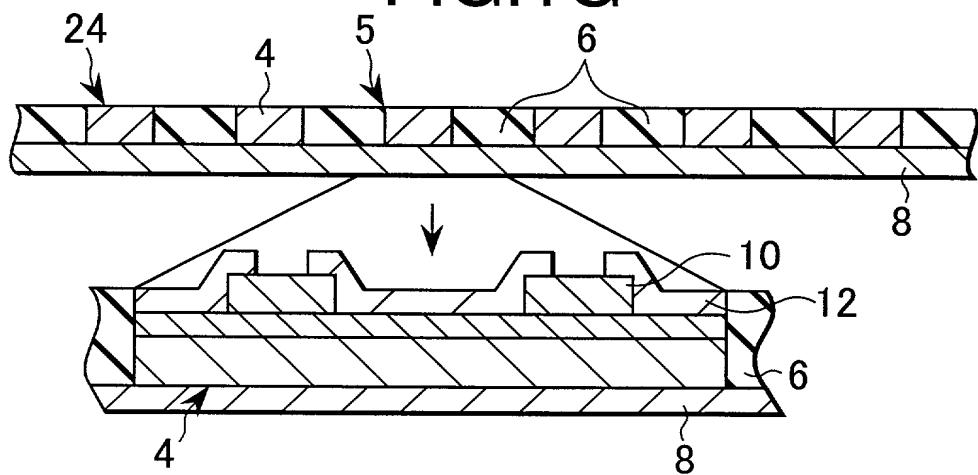


FIG.1H

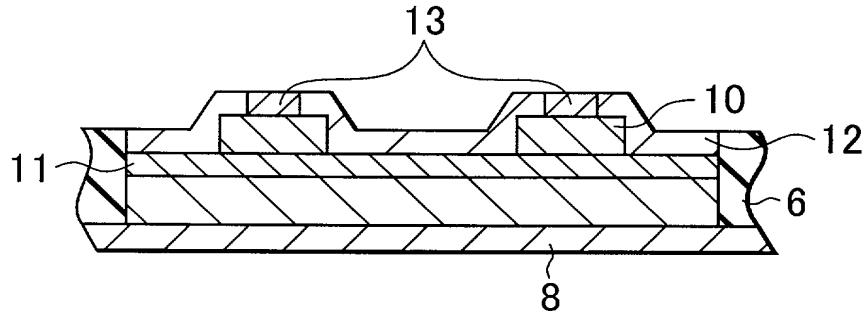


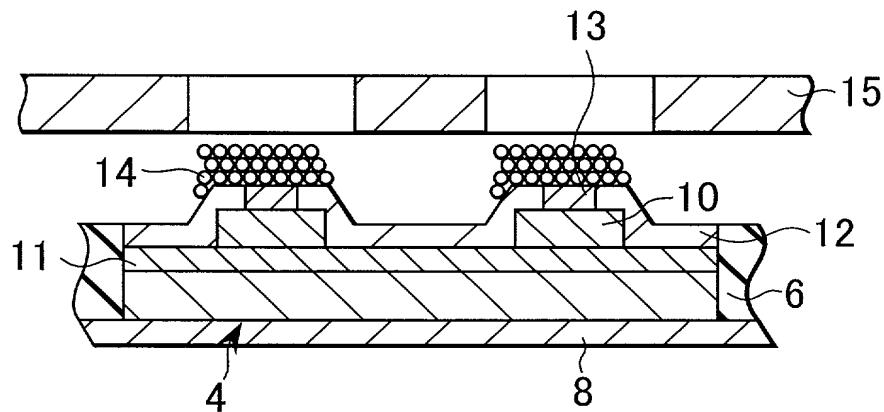
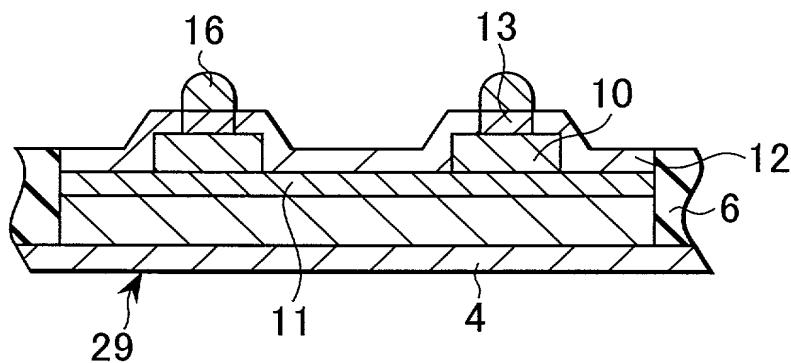
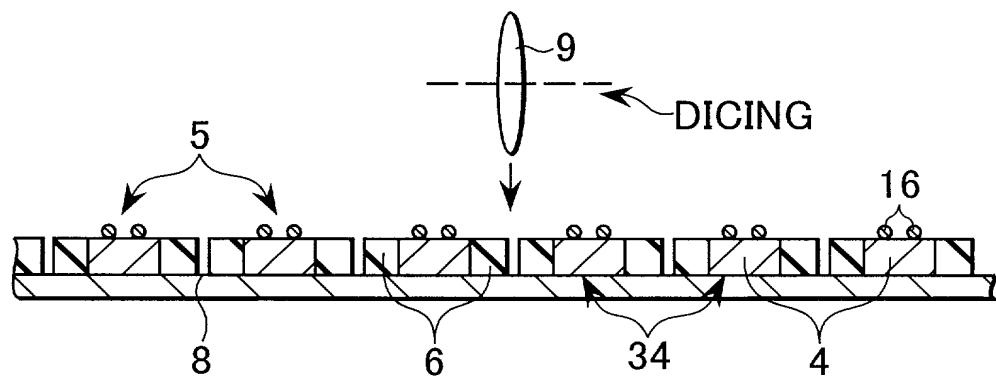
FIG.1I**FIG.1J****FIG.1K**

FIG.2

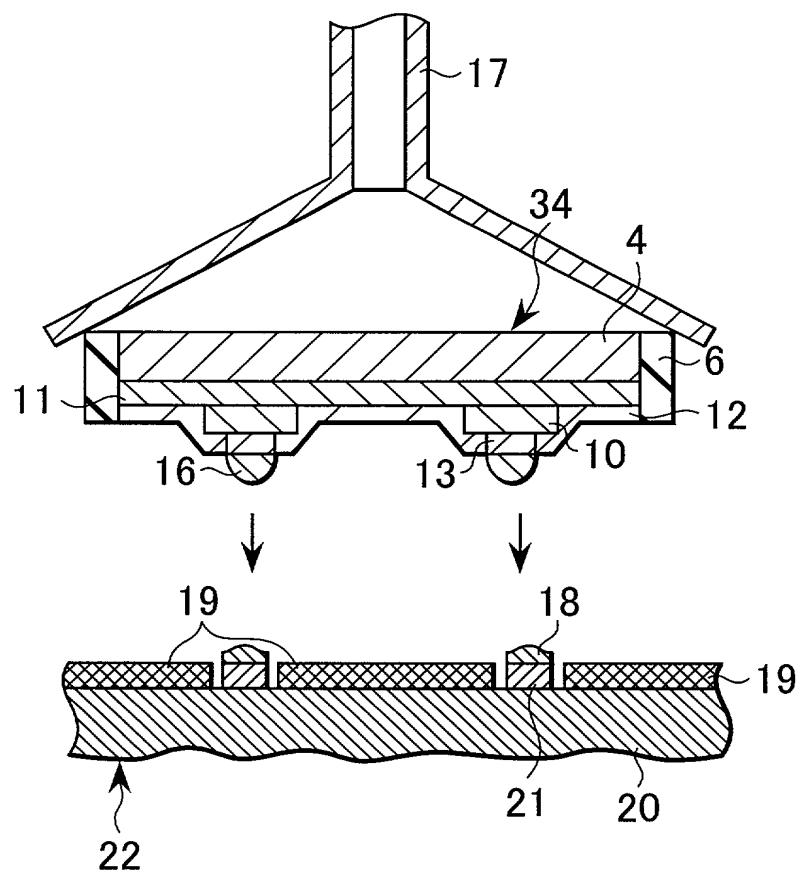


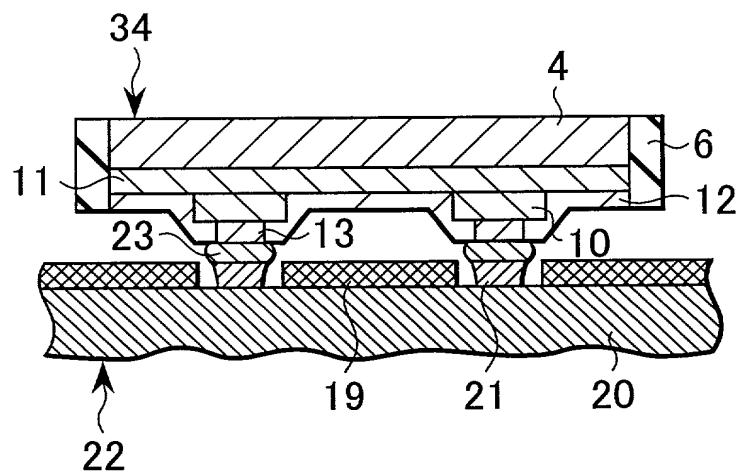
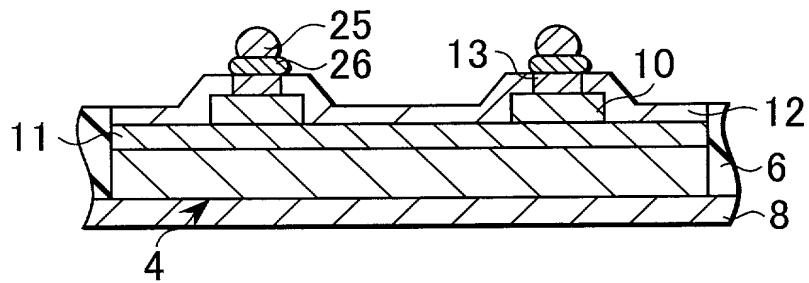
FIG.3**FIG.4**

FIG.5

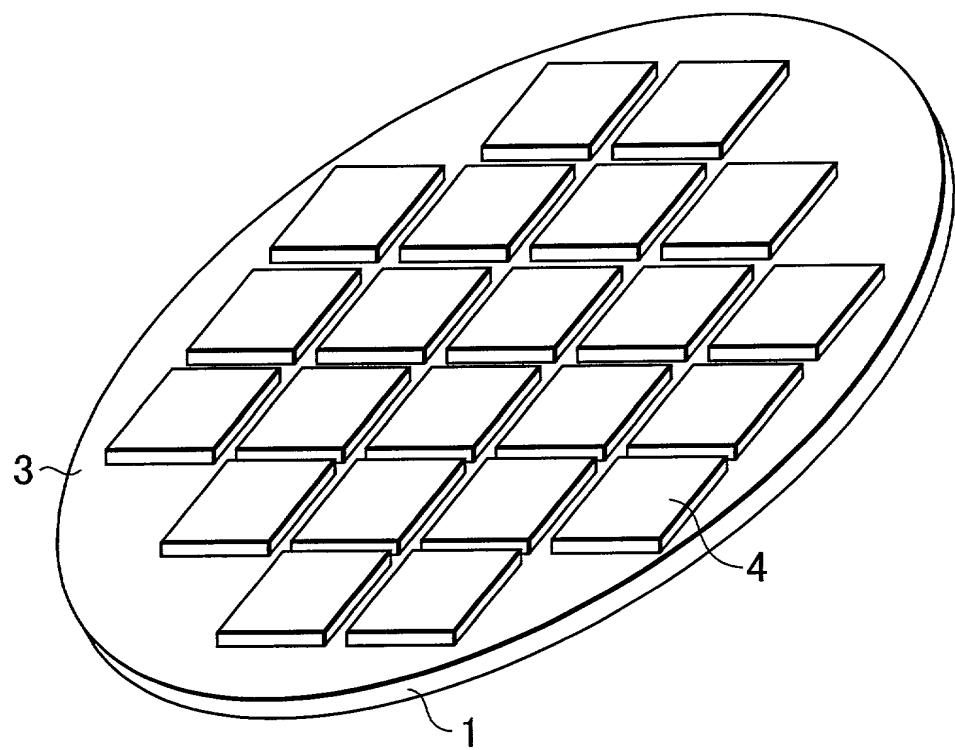


FIG.6

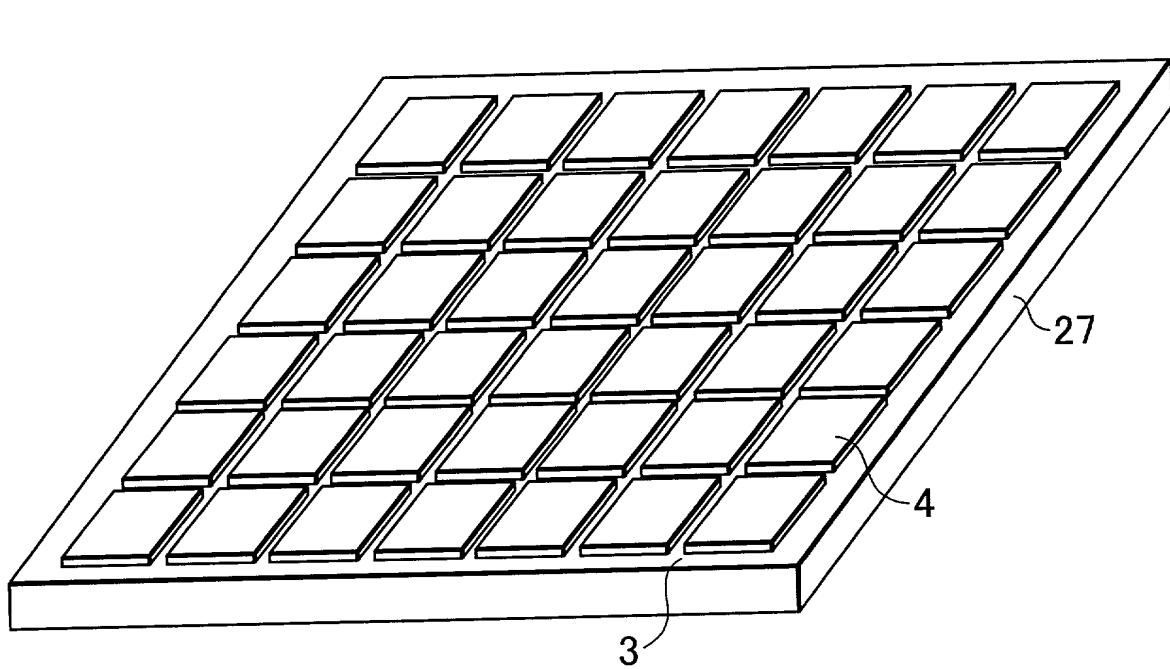


FIG.7

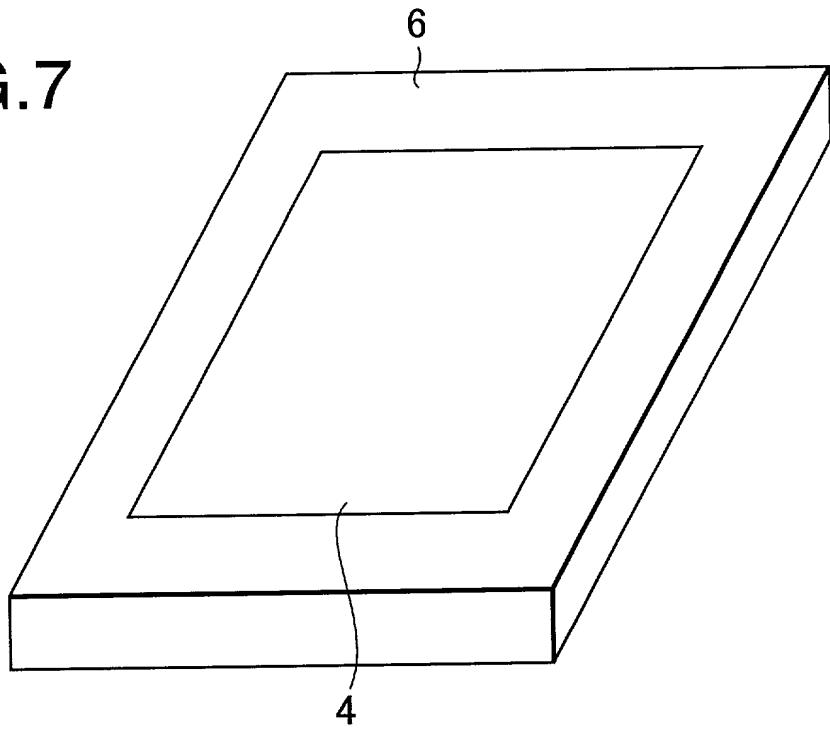


FIG.8

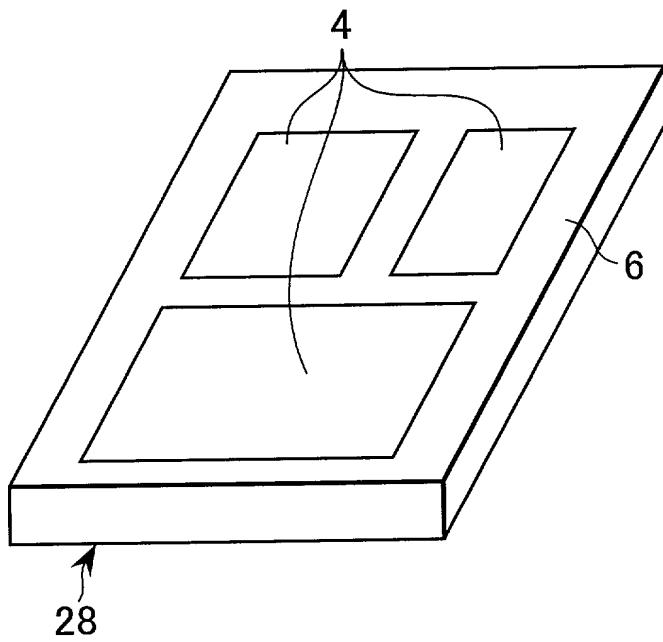
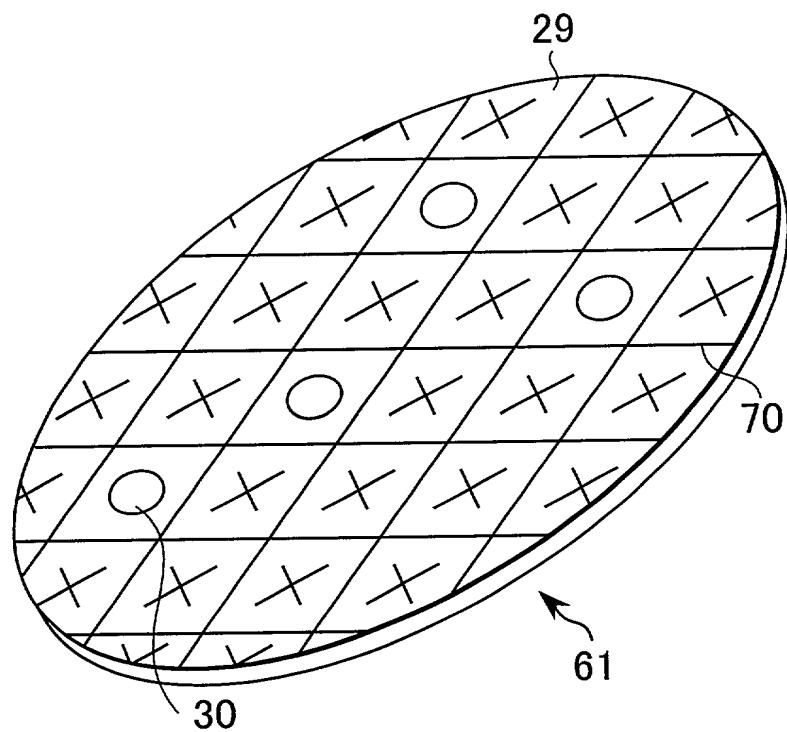


FIG.9



○:NON-DEFECTIVE CHIP

X:DEFECTIVE CHIP

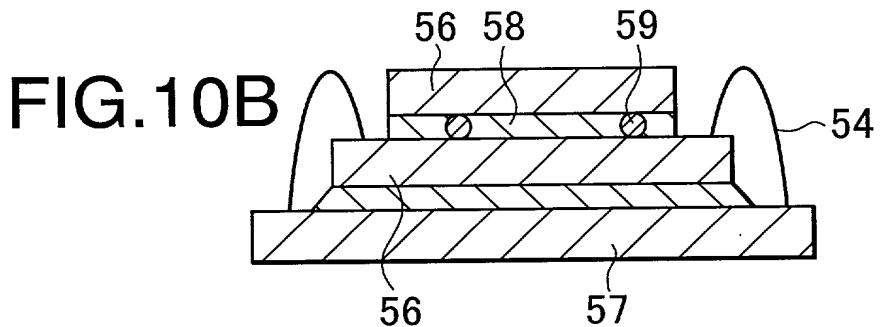
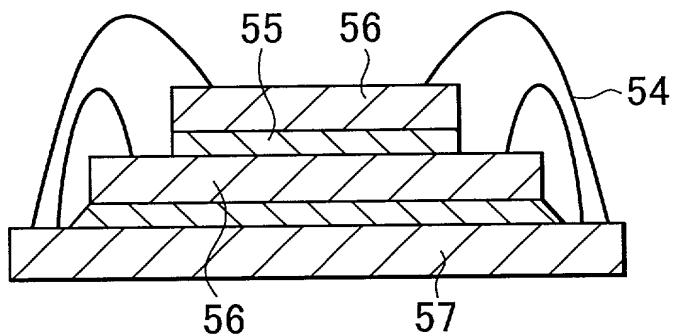
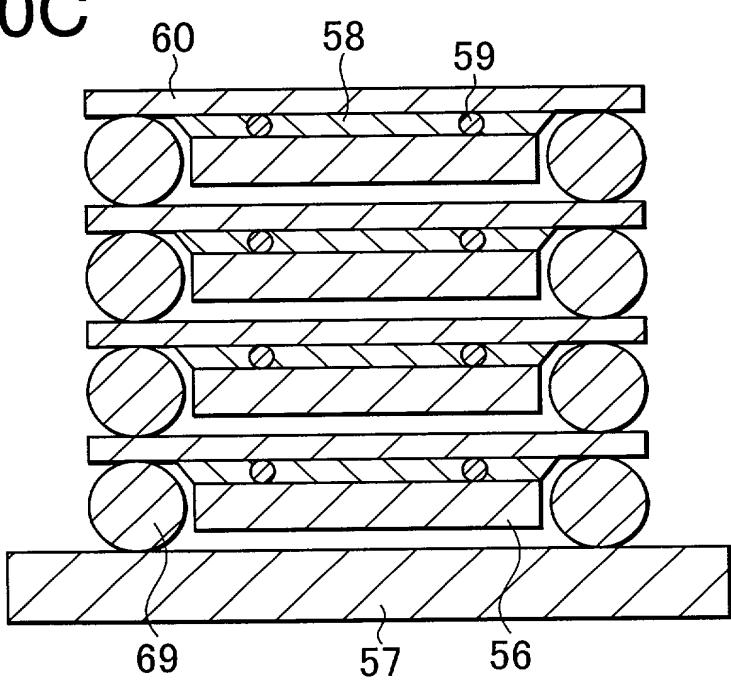
FIG.10A**FIG.10C**

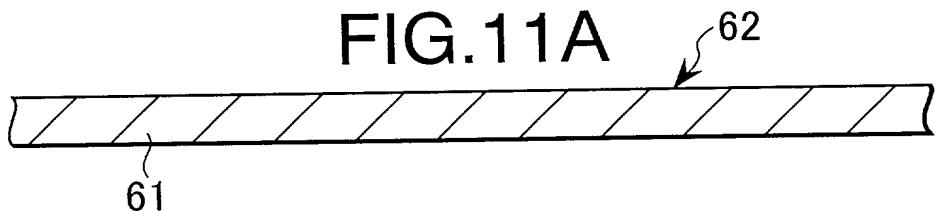
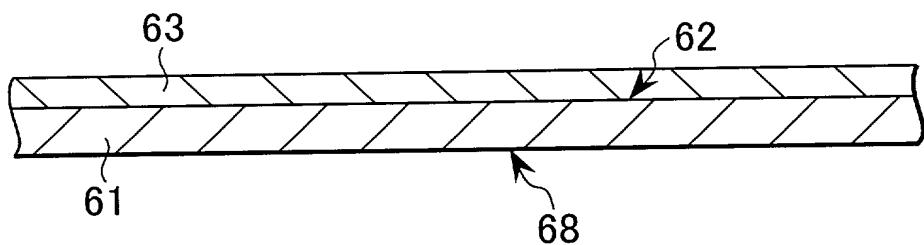
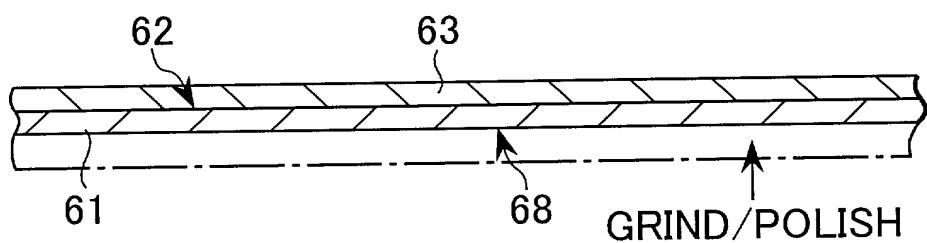
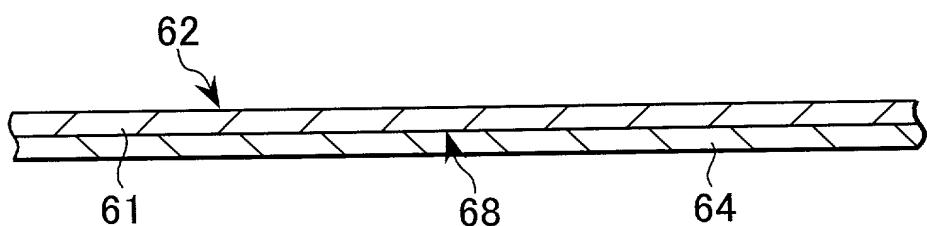
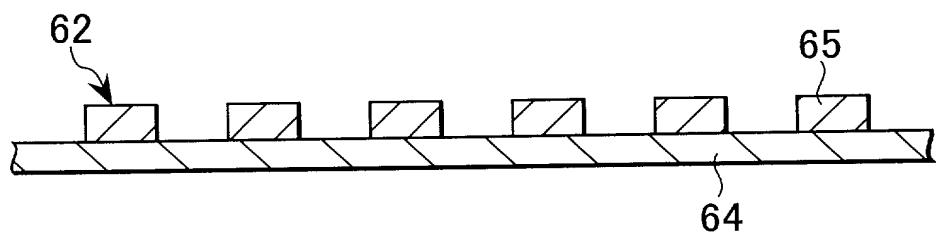
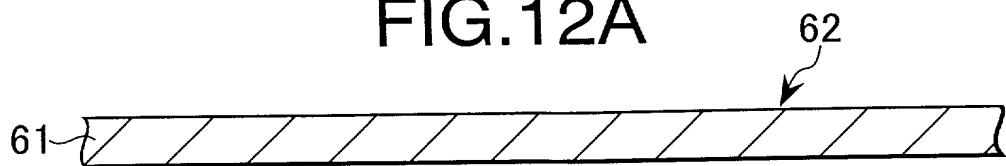
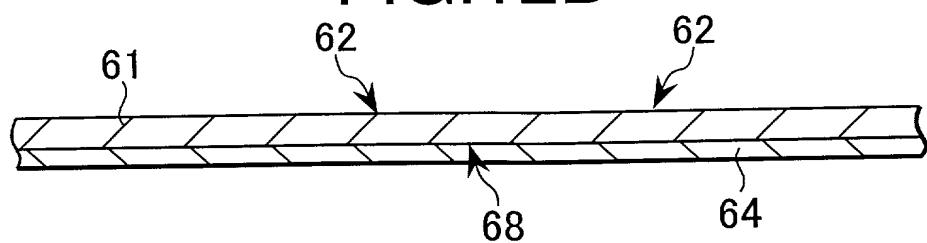
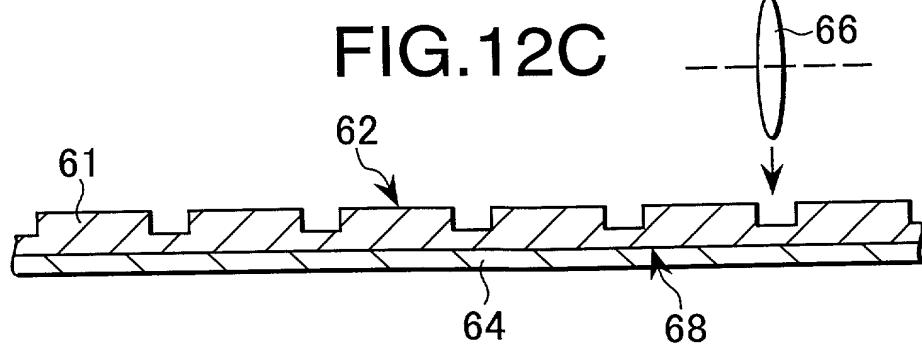
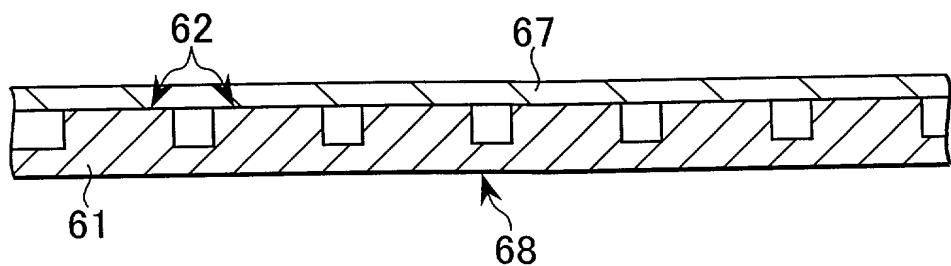
FIG.11A**FIG.11B****FIG.11C****FIG.11D****FIG.11E**

FIG.12A**FIG.12B****FIG.12C****FIG.12D****FIG.12E**